REMARKS

Claims 6, 10-13, 15 and 16 are pending Claims 6, 10 and 13 are amended, claims 8 and 9 are canceled without prejudice or disclaimer, and new claims 15 and 16 are added. A marked-up version showing the changes made to the claims by the present amendment is attached hereto as **"Version with markings to show changes made."**

Claims 6, 9 and 13 were rejected under USC § 102(e) as being anticipated by Ito et al. Further, claim 8 was rejected under 35 USC § 103(a) as being unpatentable over Ito et al. in view of Maiti et al. Favorable reconsideration of this rejection is earnestly solicited.

Contrary to Ito et al., the present invention does not use NH_3 or N_2O but uses NO for introducing N into an oxide film as set forth in amended claim 6. The problem associated with the use of NH_3 was discussed in the previous response. The use of N_2O, on the other hand, raises the problem of too strong oxidation at the time of the nitridation process. Because of the strong oxidation caused by N_2O, the amount of the N atoms incorporated into the oxide film is relatively small and the N atoms thus introduced tend to enter deeply into the oxide film. In order to introduce the N atoms with sufficient concentration, it is therefore necessary to conduct an extensive nitridation process, while such an extensive nitridation process conducted by N_2O tends to invite bird's beak formation due to the excessive oxidation of the Si substrate.

Contrary to Ito et al., the present invention uses NO for the thermal annealing process. By using NO, the problem of too strong oxidation is successfully avoided and it becomes possible to introduce a large amount of N atoms for terminating the dangling bonds in the gate oxide film.

Maiti et al. is applied by the Examiner for its disclosure of NO. However, as noted above, the use of NO would not have been obvious. That is, by using NO, the problem of too strong oxidation is successfully avoided and it becomes possible to introduce a large amount of N atoms for terminating the dangling bonds in the gate oxide film. The combination of references fails to teach or suggest the presently claimed invention.

Claims 10-12 were rejected under 35 USC § 102(e) as being anticipated by Arai et al. Favorable reconsideration of this rejection is earnestly solicited.

Arai et al. teaches a process that introduces N atoms selectively into the edge part of the gate oxide film and further into the Si substrate by way of ion implantation process. In Arai et al., it is further noted that the ion implantation process of N is conducted prior to the ion implantation process of the impurity element.

According to the process of Arai et al., the N atoms introduced by the ion implantation process escape easily from the oxide film when the impurity element is introduced by an ion implantation process conducted later. In order to minimize the escaping of the N atoms, the ion implantation process of the N atoms of Arai et al. is not and cannot be accompanied with thermal annealing process, which is usual in an ion implantation process. Thus, it is necessary that the ion implantation of the impurity element such as As+ is conducted immediately after the ion implantation process of N in Arai et al. However, the gate oxide film of Arai et al. thus subjected to repeated ion implantation process tends to accumulate substantial damage therein, and the reliability of the MOS device is deteriorated even after a thermal annealing process is conducted.

In the present invention, on the other hand, the process of introducing the N atoms comprises the steps of ion implantation of the N atoms and thermal annealing for recovering the damage, as set

forth in amended claim 10. By doing so, the gate oxide film of the present invention shows an excellent reliability particularly at the edge part of the gate electrode.

According to the feature of the present invention as set forth in new claim 15, it becomes possible to conduct the process of introducing the N atoms and the process of forming the CVD-oxide film efficiently in the same processing apparatus while minimizing the temperature difference between the step of introducing the N atoms and the step of depositing the CVD-oxide film. As a result of the reduced temperature difference between the step of introducing the N atoms and the step of depositing the CVD-oxide film, it becomes possible to minimize the thermal stress induced in the oxide film or in the CVD-oxide film. Thereby, the degree of freedom at the time of designing the semiconductor device is improved, and the yield of production of the semiconductor device is improved also.

For at least the foregoing reasons, the claimed invention distinguishes over the cited art and defines patentable subject matter. Favorable reconsideration is earnestly solicited.

Should the Examiner deem that any further action by applicants would be desirable to place the application in condition for allowance, the Examiner is encouraged to telephone applicants' undersigned attorney.

In the event that this paper is not timely filed, applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees which may be due with respect to this paper, may be charged to Deposit Account No. 01-2340.

Respectfully submitted,

ARMSTRONG, WESTERMAN, HATTORI, McLELAND & NAUGHTON, LLP

Stephen G. Adrian
Attorney for Applicants
Reg. No. 32,878

Attachments: **Version with markings to show changes made**
Petition for Extension of Time

Attorney Docket No. 970901A
Suite 1000, 1725 K Street
Washington, D.C. 20006
Tel: (202) 659-2930
Fax: (202) 887-0357
SGA/arf

VERSION WITH MARKINGS TO SHOW CHANGES MADE (09/428,052)

Claims 6, 10 and 13 have been amended as follows:

6. (Twice Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming a gate electrode pattern on said gate oxide film; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask,

wherein said step of introducing N atoms into said gate oxide film comprises a thermal annealing process of said gate oxide film conducted in an atmosphere containing [N atoms and O atoms] NO,

said thermal annealing process being conducted at a temperature of about 800°C.

10. (Three Times Amended) A method of fabricating a semiconductor device, comprising the steps of:

forming a gate oxide film on a substrate;

forming a gate electrode pattern on said gate oxide film; and

introducing N atoms into said gate oxide film while using said gate electrode pattern as a mask,

wherein said step of introducing N atoms into said gate oxide film [includes] comprises the steps of conducting an ion implantation process of N ions; and applying a thermal annealing process to said gate oxide film.

13. (Amended) A method as claimed in claim 6, further comprising the step of forming diffusion regions in said substrate at both lateral sides of said gate electrode pattern by introducing impurity elements into said substrate through said gate oxide film while using said gate electrode pattern as a mask, and wherein said step of introducing impurity elements is conducted prior to said step of introducing N atoms into said gate oxide film.